|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **LEADLAG- in case of DC INPUT(slow dc with 100Hz & 50Hz frequency)** | | | | | | |
| **Various Detected Faults in LEADLAG in the presence of faults with deviations ( >5%)** | | | | | | |
| **Injected Faults** | **=500,**  **=5.1931e-04**  **Optimal Order – 14th** | | **=1000,**  **= 5.1978e-04**  **Optimal Order – 14th** | | **=2000,**  **= 5.2020e-04**  **Optimal Order – 14th** | |
| **No. of Coefficients Out of Bound** | **Fault Detection Status** | **No. of Coefficients Out of Bound** | **Fault Detection Status** | **No. of Coefficients Out of Bound** | **Fault Detection Status** |
| R1 3%**↑** | **1** | **√** | **1** | **√** | **1** | **√** |
| R2 2% **↓** | 1 | **√** | **1** | **√** | **0** | **X** |
| R3 4% **↑** | **0** | **X** | **0** | **X** | **0** | **X** |
| C1 2% **↓** | **0** | **X** | **0** | **X** | **0** | **X** |
| C2 4% **↑** | **0** | **X** | **0** | **X** | **0** | **X** |
| R1 1%**↓** | **0** | **X** | **0** | **X** | **0** | **X** |
| R2 1%**↑** | **0** | **X** | **0** | **X** | **0** | **X** |
| R3 4% **↓** | 1 | **√** | **0** | **X** | **0** | **X** |
| C1 3% **↑** | **0** | **X** | **0** | **X** | **0** | **X** |
| C2 4% **↓** | **0** | **X** | **0** | **X** | **0** | **X** |